RECEIVER DECODING ALGORITHM TO ALLOW HITLESS
N+1 REDUNDANCY IN A SWITCH

FIELD OF THE INVENTION

The present invention is related to a switch having
5   fabrics that can recover from the failure of a single fabric. More
specifically, the present invention is related to a switch having
fabrics that can recover from the failure of a single fabric with
the aid of a check sum that is added to parity data which is
striped onto the fabrics of the switch.

10   ## BACKGROUND OF THE INVENTION

A switch which stripes data onto multiple fabrics and
sends parity data to another fabric has been described in U.S.
patent application serial number 09/333,450, incorporated by
reference herein. See also U.S. patent application serial number
15   09/293,563 which describes a wide memory TDM switching system,
incorporated by reference herein. The present invention describes
the receiver algorithm used in a data communications system which
allows for detection/recovery of data and close to hitless recovery
of a single element in a switch.

20   The present invention allows a switch that utilizes
striping to tolerate a single hardware failure without requiring a
change-over time.   Conventional redundancy systems require
detection of bad data and reconfiguration of the switch to an
alternate source of data.   The time between the failure to the
25   successful reconfiguration of the system results in lost data which
impacts traffic going through the switch.   The technique of the
present invention will have only a small portion of the traffic